REMARKS

In the Office Action dated May 4, 2007, the Examiner rejected claims 1-15 under 35 USC 112, second paragraph, rejected claims 1-3, 9 and 10 under 35 USC 102 as anticipated by Nakaya in US Patent 6,188,240 and rejected claims 1, 14 and 15 under 35 USC 102 as anticipated by New in US Patent 6,154,053. In response thereto, the Applicants have amended claims 1, 5, 8 and 15. Claims 1-15 remain at issue.

Status Inquiry of Claims 4-8 and 11-13

In the Office Action, the Examiner rejected claims 1-3, 9 and 10 under 35 USC 102 as anticipated by Nakaya and claims 1, 14 and 15 under 35 USC 102 as anticipated by New. Claims 4-8 and 11-13, however, were not anticipated by either Nakaya or New. These claims were rejected only under 35 USC 112, second paragraph, by virtue of their dependency on claim 1. Due to the lack of a formal rejection on the merits of claims 4-8 and 11-13, the Applicants assume that these claims are allowable, provided that (i) they are written in independent form; and (ii) the 35 USC 112, second paragraph issue with claim 1 is addressed. The Applicants request a confirmation of the Applicants assumption.

The Art Rejection

The Examiner has rejected certain claims as separately anticipated by Nakaya and New. The Applicants strongly disagree. Neither reference anticipates the present invention as claimed.

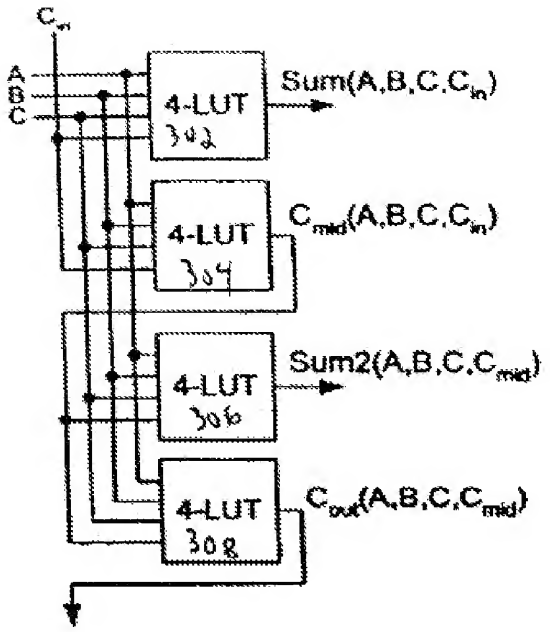
Certain claims of the present application cover a logic element in a PLD having a K-input LUT that is capable of generating **binary result signals** which are indicative of **at least two stages** in the LUT, which are configured to **arithmetically combine the binary input signals** provided to the LUT. In contrast as described in detail below, the equivalent logic elements in Nakaya and New are each capable of generating only a ***single*** arithmetic or binary output.

With reference to Figure 17, the logic blocks 2 of Nakaya are capable of generating only a single arithmetic (i.e., "binary") or sum output "S". The other output of each block 2 is the carry output "C", which is not the equivalent of a second binary output. With reference to column 15 lines 40-45, Nakaya clearly defines the signal "C" as a "***core output signal***" and the signal "S" as a "***summed output signal***". The carry or C signal is therefore ***not*** a binary result signal.

With reference to Figure 14, New discloses a block diagram of a Complex Logic Block (CLB) 1401. The CLB 1401 includes a plurality of logic cells 1411-1414. Each logic cell 1411-1414 includes a function generator 401, carry/control logic 411 and a register 412. See column 11 lines 25-35. The CLB 1401, logic cells 1411-1414, and function generators 401 in New are the equivalent of the Applicant's "LAB", logic element or "LE", and K-input LUT in the present application respectively.

Each logic cell 1411-1414 generates a ***single*** carry signal C (designated as Cin), which is part of a carry chain and which is applied to the next logic cell, and a ***single*** arithmetic or binary output S. As taught in column 1 lines 44-45, the S signal is the arithmetic sum of signals A, B and Cin applied to each logic cell. New therefore does ***not*** teach a logic element (or logic cell) that is capable of generating **two binary result signals**.

Lastly, for the sake of comparison, the logic element of Figure 4 of the present application is provided below. As illustrated in this embodiment, the logic element is capable of generating two binary result signals, Sum(A, B, C, Cin) and Sum2(A, B, C, Cmid), as well as two carry signals Cmid and Cout.



400

Figure 4

The logic cells of both Nakaya and New, as detailed above, are incapable of generating two binary result signals as provided and claimed with the present invention (e.g., Sum and Sum2).

It should be noted that the use of Figure 4 herein is for illustrative purposes and in no way should be construed as limiting the invention. As noted in the specification, the present invention covers a logic element that is capable of generating two or more binary result signals.

The Applicants believe that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution, the undersigned can be reached at the telephone number set out below.

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